



JPL

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

UI, Norihiko, et al.

Group Art Unit: **2822**

Serial No.: **10/618,717**

Examiner: **Kiesha L. ROSE**

Filed: **July 15, 2003**

P.T.O. Confirmation No.: **7409**

For: **FIELD-EFFECT TRANSISTOR AND METHOD OF PRODUCING THE SAME**

RESPONSE TO THE RESTRICTION REQUIREMENT
DATED December 9, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: January 4, 2005

Sir:

This paper is submitted in response to the Official Action dated **December 9, 2004**.

In the Action, restriction is required between Group (I), Claims 1-8; and Group (II),
Claims 9-18.

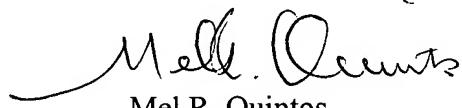
Applicants hereby elect the subject matter of Group (I), Claims 1-8, for prosecution in
this application. This election is made without traverse, it being understood that the applicants'
rights to the filing of a divisional application directed to the non-elected subject matter under 35
USC 120 and 35 USC 121 are retained.

In the event that this paper is not timely filed, applicants hereby petition for an
appropriate extension of time. The fee for any such extension may be charged to our Deposit
Account No. 01-2340.

In the event any additional fees are required in connection with this response, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP



Mel R. Quintos
Attorney for Applicants
Reg. No. 31,898

MRQ/lrj
Atty. Docket No. 030864
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930



23850
PATENT TRADEMARK OFFICE